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PTO/SB/21 (08-00)

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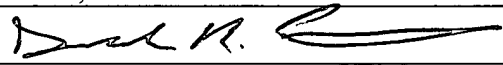
Application Number	09/886,972
Filing Date	June 25, 2001
First Named Inventor	Yoshihisa KATO et al.
Group Art Unit	2818
Examiner Name	Ly D. PHAM
Attorney Docket Number	740819-566

Total Number of Pages in This Submission

ENCLOSURES (check all that apply)

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Remarks		<input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 19-2380 for the above identified docket number.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Donald R. Studebaker, Reg. No. 32,815 Nixon Peabody LLP 8180 Greensboro Drive Suite 800 McLean, VA 22102
Signature	
Date	March 14, 2003

CERTIFICATE OF MAILING

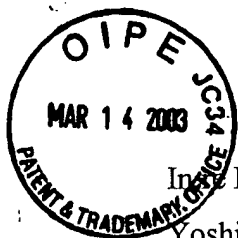
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor Patent Application of:)
Yoshihisa KATO et al.) Group Art Unit: 2818
Serial No. 09/886,972) Examiner: Ly D. PHAM
Filed: June 25, 2001)
For: SEMICONDUCTOR MEMORY AND) Date: March 14, 2003
METHOD FOR DRIVING THE SAME)

7/Response
G. Stanley
3-18-03

REQUEST FOR RECONSIDERATION

Commissioner for Patents
Washington, D.C. 20231

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In response to the Office Action mailed December 16, 2002, please consider Applicants' following remarks in connection with the above-identified application.

REMARKS

The Office Action December 16, 2002 was received and reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

Claims 1-4 are pending in the present application, of which claims 3 and 4 have been withdrawn from consideration in a response to an election requirement dated October 8, 2002.

Referring now to the detailed Office Action, claim 1 stand rejected under 35 U.S.C. §102(e) as anticipated by Taira (U.S. Patent No. 6,049,477), and claim 2 stand rejected under 35 U.S.C. §103(a) as unpatentable over Taira in view of Ishiwara (U.S. Patent No. 6,362,500). Both of these rejections have been previously applied for the same reasons as stated in the Office Action of June 14, 2002. Applicants respectfully traverse these rejections at least for the reasons provided below.

One of the main features of the invention in the claim 1 or 2 resides in the magnitude of the data read voltage applied between the drain and the source of the FET (field effect transistor)